SPECIFICATION
FOR

Module:YS-T078402 (V1.0)

Designed by	R&D Checked by	Quality Department by	Approved by

Approval by Customer:

OK

NG, Problem survey

Approved By_____

Revision Record

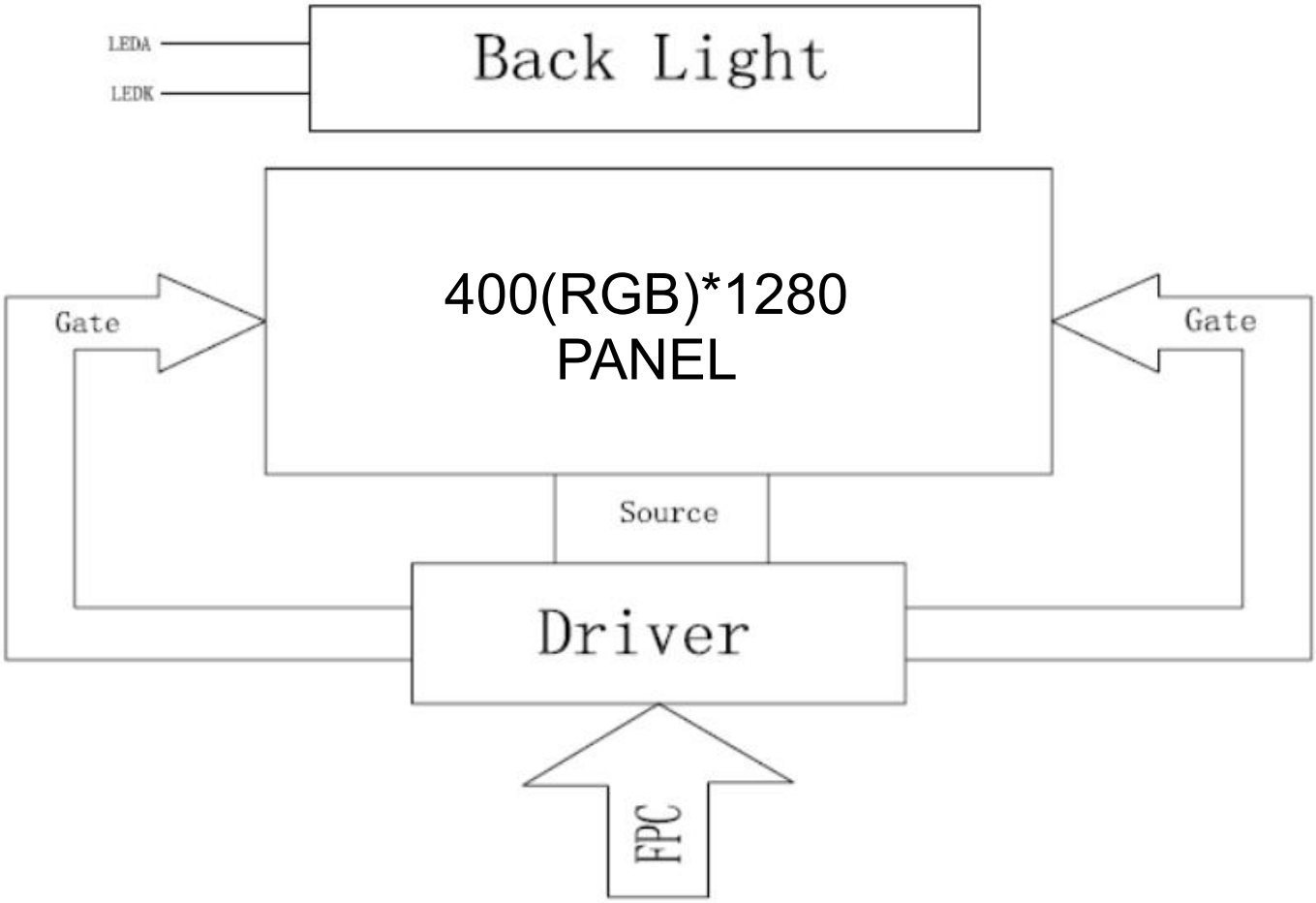
REV NO.	REV DATE	Contents Before Change	Contents After Change	Note
V1.0	2022/08/01	NEW ISSUE By PAN;		

Contents

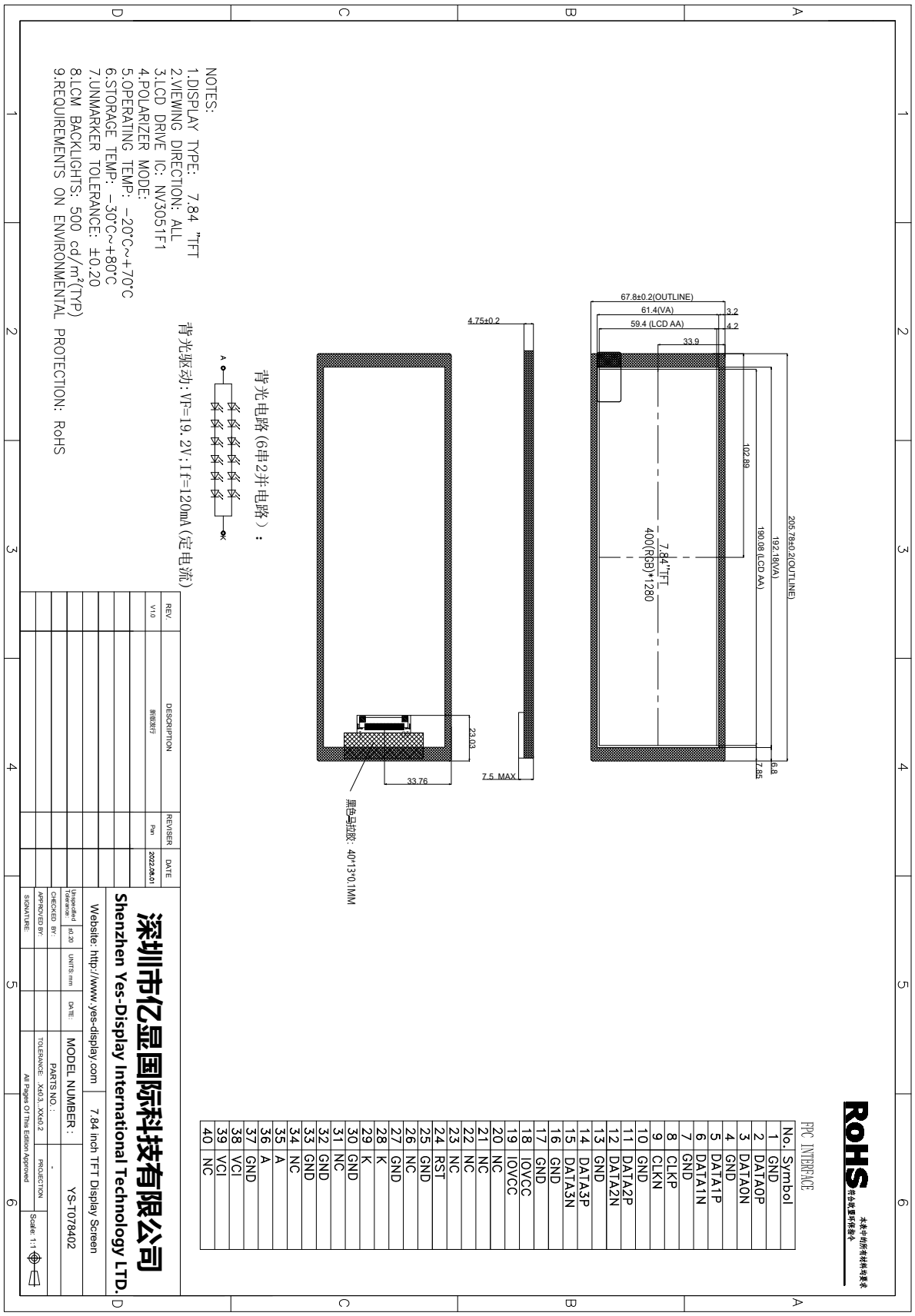
1. Technical parameters

ITEM	STANDARD VALUES	UNITS
LCD type	7.84 TFT	--
Dot arrangement	400(RGB)×1280	dots
Color filter array	RGB vertical stripe	--
Display mode	IPS / Transmission / Normally Black	-
Eyes Viewing Direction	ALL	--
Driver IC	NV3051F1	--
Module size	205.78(W)×67.80(H)×7.5(T)(Exclude FPC)	mm
Active area	190.08(W)×59.40(H)	mm
Interface	MIPI	--
Operating temperature	-20 ~ +70	°C
Storage temperature	-30 ~ +80	°C
Back Light	White LED*6 *2（Dual chip）	--

2. Block Dimension



3. Outline Dimension



4. Input terminal Pin Assignment Description

4.1 TFT Pin Description

PIN NO.	PIN NAME	DESCRIPTION
1	GND	Power ground
2	DATA_0P	DATA0+ differential data signals.
3	DATA_0N	DATA0- differential data signals.
4	GND	Power ground
5	DATA_1P	DATA1+ differential data signals.
6	DATA_1N	DATA1- differential data signals.
7	GND	Power ground
8	CLKP	CLK+ differential clock signals
9	CLKN	CLK- differential clock signals.
10	GND	Power ground
11	DATA_2P	DATA2+ differential data signals.
12	DATA_2N	DATA2- differential data signals.
13	GND	Power ground
14	DATA_3P	DATA3+ differential data signals.
15	DATA_3N	DATA3- differential data signals.
16-17	GND	Power ground
18-19	IOVCC	Power supply for IO analog
20-23	NC	NC
24	RST	Reset pin. Initializes the IC, when this signal is low. Must be reset after power is stable.
25	GND	Power ground
26	NC	NC
27	GND	Power ground
28-29	LEDK	Power supply for backlight cathode input terminal.
30	GND	Power ground
31	NC	NC
32-33	GND	Power ground
34	NC	NC
35-36	LEDA	Power supply for backlight anode input terminal.
37	GND	Power ground
38-39	VCI	Power supply for analog
40	NC	NC

5. LCD Optical Characteristics

Item	Symbol		Condition	Min.	Typ.	Max.	Unit	Note
Brightness	Bp		θ=0° Φ=0°	400	450	-	cd/m²	1
Uniformity	⊿Bp			75	80	-	%	1,2
Viewing Angle	3:00		Cr≥10	-	80	-	Deg	3
	6:00			-	80	-		
	9:00			-	80	-		
	12:00			-	80	-		
Contrast Ratio	Cr		θ=0° Φ=0°	700	900		-	4
Response Time	T_r+T_f				30	35	ms	5
Color of CIE Coordinate	W	x	θ=0° Φ=0°	-0.05	0.26	+0.05	-	1,6
		y			0.27		-	
	R	x			0.623		-	
		y			0.329		-	
	G	x			0.280		-	
		y			0.599		-	
	B	x			0.148		-	
		y			0.062		-	
NTSC Ratio	S			65	70	-	%	

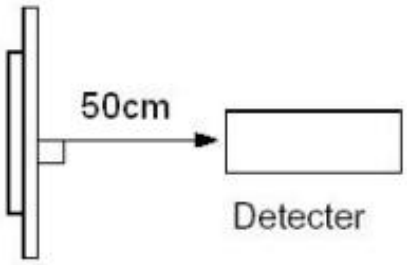
Note：The parameter is slightly changed by temperature, driving voltage and materiel

Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment BM-7 (Φ7.5mm)

Measuring condition:

- Measuring surroundings: Dark room.
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.

Measured value at the center point of LCD panel after more than 5 minutes while backlight turning on.

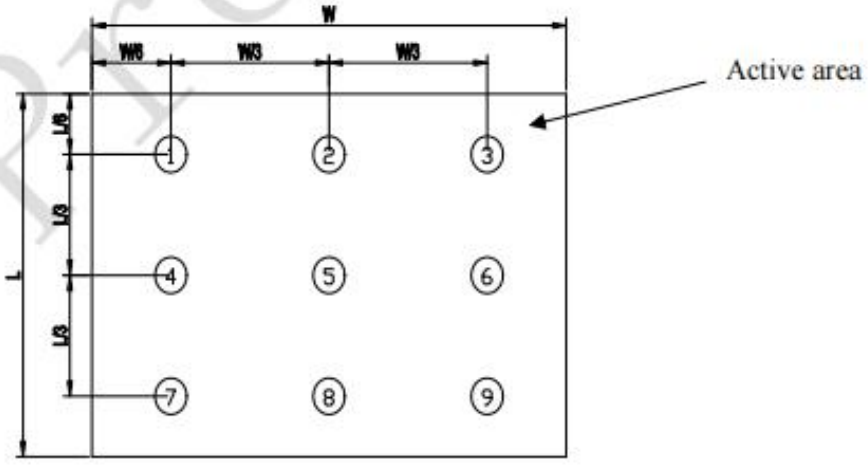


Note 2: The luminance uniformity is calculated by using following formula.

⊿Bp = Bp (Min.) / Bp (Max.)×100 (%)

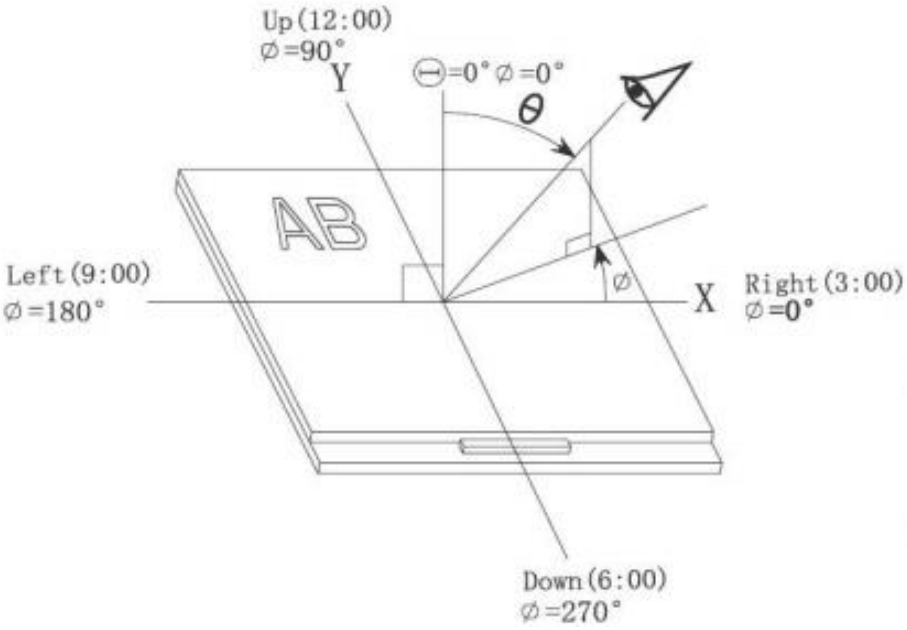
Bp (Max.) = Maximum brightness in 9 measured spots

Bp (Min.) = Minimum brightness in 9 measured spots.

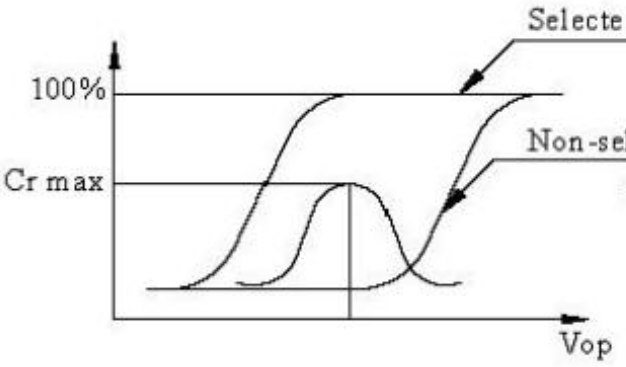


Note 3: The definition of viewing angle:

Refer to the graph below marked by θ and Φ



Note 4: Definition of contrast ratio.(Test LCD using DMS501)



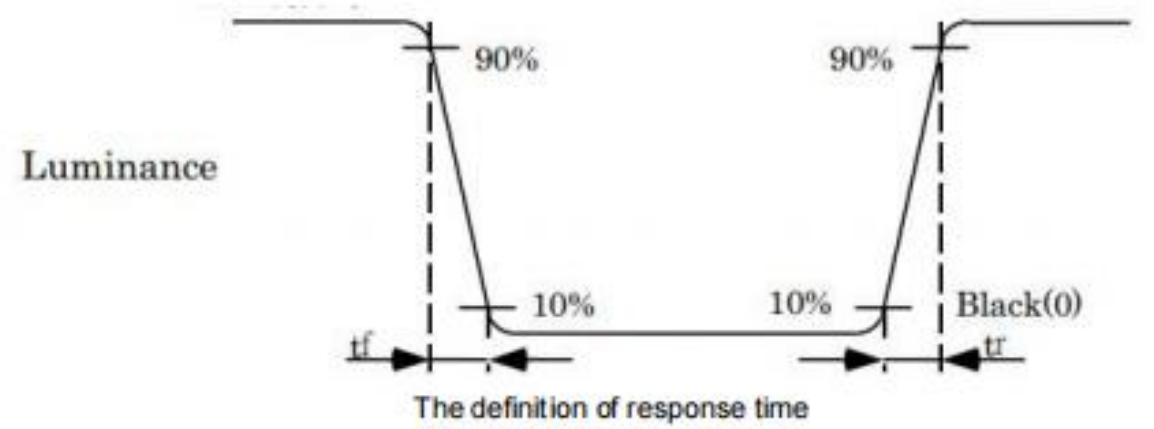
*Conditions

Operating Voltage	:	Vop
Frame Frequency	:	70Hz
Appling Waveform	:	1/N duty 1/a bias
View angle (θ, Φ)	:	(0°, 0°)

$$Contrast\ ratio(Cr) = \frac{Brightness\ of\ selected\ dots}{Brightness\ of\ non-selected\ dots}$$

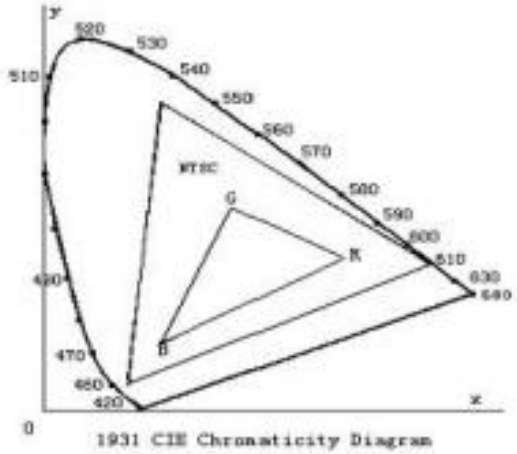
Note 5: Definition of Response time. (Test LCD using DMS501):

The output signals of photo detector are measured when the input signals are changed from "black" to "white"(Tf) and from "white" to "black"(Tr), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.Refer to figure as below.



The definition of response time

Note 6: Definition of Color of CIE Coordinate and NTSC Ratio.



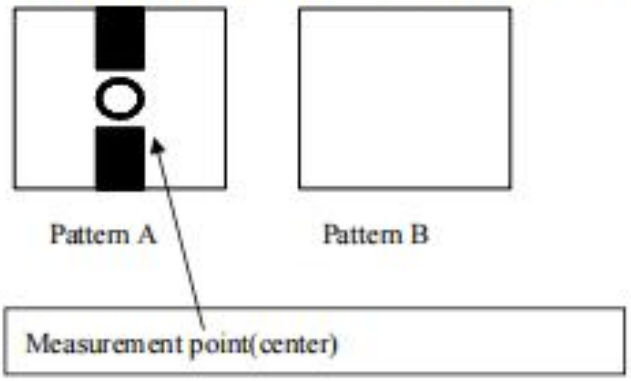
1931 CIE Chromaticity Diagram

Color gamut:

$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 7: Definition of cross talk.

Cross talk ratio(%)=|pattern A Brightness-pattern B Brightness|/pattern A Brightness*100



Electric volume value=3F+/-3Hex

6. TFT Electrical Characteristics

6.1 Absolute Maximum Ratings

(VCI=2.5V~6.0V, IOVCC = 1.65V~3.6V, Ta = -30℃ ~ 85℃)

Parameter	Symbol	Rating	Unit	Note
Power Supply Voltage 1	IOVCC-VSS	-0.3 ~ +4.5	V	
Power Supply Voltage 2	VDDAM-VSS	-0.3 ~ +6.6	V	
Power Supply Voltage 3	VCI-VSS	-0.3 ~ +6.6	V	
Power Supply Voltage 4	VPP-VSS	-0.3 ~ +7.8	V	
Power Supply Voltage 5	DVDD-VSS	-0.3 ~ +1.8	V	
Power Supply Voltage 6	VSP-VSS	-0.3 ~ +6.6	V	
Power Supply Voltage 7	VSS-VSN	-0.3 ~ +6.6	V	
Power Supply Voltage 8	VGH-VGL	-0.3 ~ +32	V	
Input Voltage	Vt	-0.3 ~ IOVCC +0.3	V	
Operating Temperature	Topr	-30 ~ +85	℃	
Storage Temperature	Tstg	-40 ~ +125	℃	

6.2 DC Characteristics

6.2.1. Basic DC characteristic

(VCI=2.5V~6.0V, IOVCC = 1.65V~3.6V, Ta = -30℃ ~ 85℃)

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VCI	Operating Voltage	2.5	2.8	6.0	V	
Logic Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.6	V	
MIPI interface operating voltage	VDDAM	MIPI supply voltage	1.75	-	6.0	V	Note1
Input/Output							
Logic High level input voltage	VIH	-	0.7*IOVCC	-	IOVCC	V	
Logic Low level input voltage	VIL	-	VSS	-	0.3*IOVCC	V	
Logic High level output voltage	VOH	IOH = -0.1mA	0.8*IOVCC	-	IOVCC	V	
Logic Low level output voltage	VOL	IOL = +0.1mA	VSS	-	0.2*IOVCC	V	
Logic Input leakage current	IIL	Vin=IOVCC or VSSI	-0.1	-	+0.1	uA	
VCOM Operation							
VCOM voltage	VCOM	-	-3.375	-1.0	0	V	
Source Driver							
Source output range	Vsout	-	VGMN+0.1	-	VGMP-0.1	V	
Gamma positive reference voltage	VGMP	-	2.64	-	5.846	V	
Gamma negative reference voltage	VGMN	-	-5.702	-	-2.509	V	
Source output settling time	Tr	Below with 99% precision	-	TBD	-	us	
Output deviation voltage (Source positive output channel)	V,dev	Sout >=+4.2V, Sout<=+0.8V	-	-	TBD	mV	
		+4.2V>Sout>+0.8V	-	-	TBD	mV	
Output deviation voltage (Source negative output channel)	V,dev	Sout <=-4.2V, Sout>=-0.8V	-	-	TBD	mV	
		-4.2V<Sout<-0.8V	-	-	TBD	mV	

Output offset voltage	VOFFSET	-	-	-	TBD	mV	
Reference Voltage							
Internal reference voltage	VREF		1.876	2.00	2.125	V	
Booster operation							
1st booster output voltage	VSP		4.5		6	V	
	VSN		-6		-4.5	V	
2ndbooster output voltage	VGH		11.0		18.0	V	
	VGL		-15.5		-7.0	V	
Current Consumption							
Sleep-IN mode	IIOVCC	RESX=High		TBD	TBD	uA	Note2
	IVCI			TBD	TBD	uA	
Deep standby mode	IIOVCC	RESX=High		TBD	TBD	uA	
	IVCI			TBD	TBD	uA	

Note1. VDDAM are used as the power of MVDD LDO, the voltage level can't be lower than 1.75V

Note2. The power/temperature conditions for Current consumption (Sleep-IN) part is (VCI, VDDAM) =3.0V, IOVCC=1.8V@25℃

(These values might be updated after further evaluation.)

6.2.2. MIPI DC character

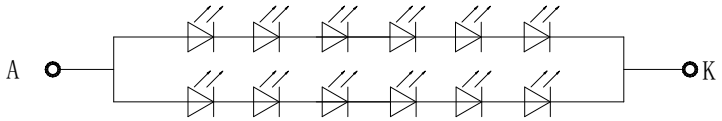
DC characteristics for MIPI-DSI

(VCI=2.5V~6.0V, IOVCC = 1.65V~3.6V, Ta = -30℃~ 85℃)

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Power supply voltage for MIPI Interface						
Power supply voltage for MIPI interface	VDDAM	-	1.75	1.8	6.0	V
	MV1P2	-	1.125	1.2	1.3	V
LPDT Input Characteristics						
Pad signal voltage range	VI	-	-50	-	1350	mV
Ground Shift	VGNDSH	-	-50	-	50	mV
Logic 0 input threshold	VIL	-	0	-	550	mV
Logic 1 input threshold	VIH	-	880	-	MV1P2	mV
Input hysteresis	VHYST	-	25	-	-	mV
LPDT Output Characteristics						
Output low level	VOL	-	-50	-	50	mV
Output high level	VOH	-	1.1	1.2	1.3	V
Logic 1 contention threshold	VILCD,MIN	-	450	-	MV1P2	mV
Logic 0 contention threshold	VIHCD,MAX	-	0	-	200	mV
Output impedence of LPDT	ZOLP	-	80	100	125	ohm
Hi-speed Input/Output Characteristics						
Single-end input low voltage	VILHS	-	-40	-	-	mV
Single-end input high voltage	VIHHS	-	-	-	460	mV
Common mode voltage	VCMRXDC	-	70	-	330	mV
Hi-speed transmit voltage	VOD	-	140	200	250	mV
Differential input impedence	ZID	-	80	100	125	ohm

6.3 LED Backlight Characteristics

背光电路(6串2并电路）：



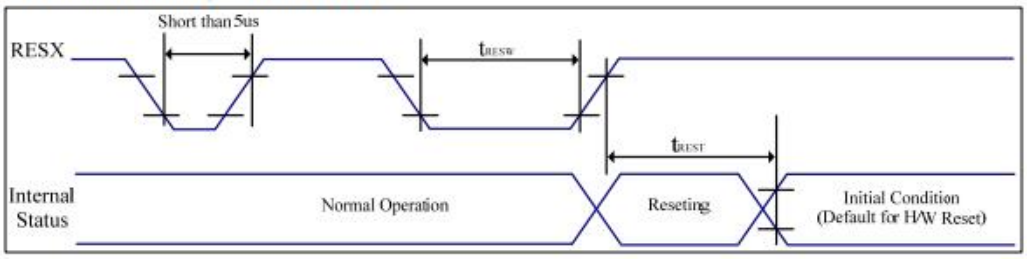
背光驱动:VF=19.2V;If=120mA(定电流)

Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition
Supply Voltage	Vf	-	19.2	-	V	If=120mA
Supply Current	If	-	120	-	mA	If=120mA
Luminous Intensity for LCM	-	-	500	-	cd/m^2	If=120mA
Uniformity for LCM	-	-	70	-	%	If=120mA
Life Time	-	-	50000	-	Hr	If=120mA
Backlight Color	White					

7. Timing Characteristics

7.1 TFT Timing Characteristics

7.1.1. Reset timing characteristics



VSS=0V, IOVCC=1.65V to 3.6V, VCI=2.5V to 6.0V,Ta = -30℃ to 85℃

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
T_{resw}	*1) Reset low pulse width	RESX	10	-	-	-	us
T_{rest}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Table: Reset input timing

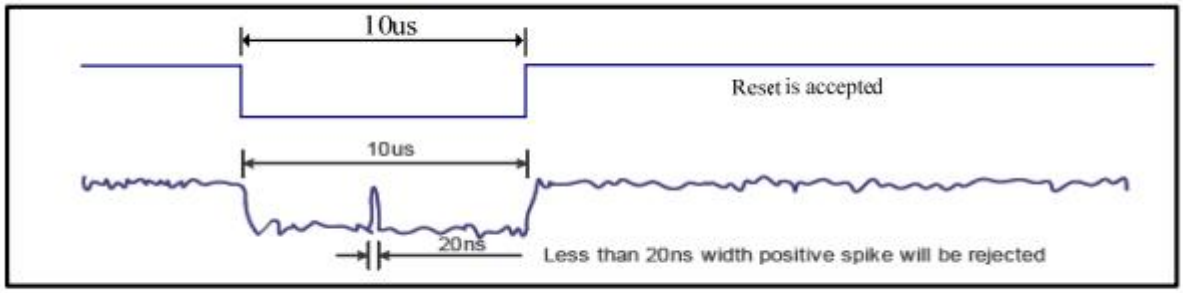
Note 1: Due to an electrostatic discharge on RESX line,spike does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode) , then return to default condition for H/W reset.

Note 3: During Reset Complete Time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register. After a rising edge of RESX, there is a H/W reset complete time (Trest) which lasted 5ms.The loading operation will be done every time during this reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

7.1.2. Serial interface characteristics (SPI)

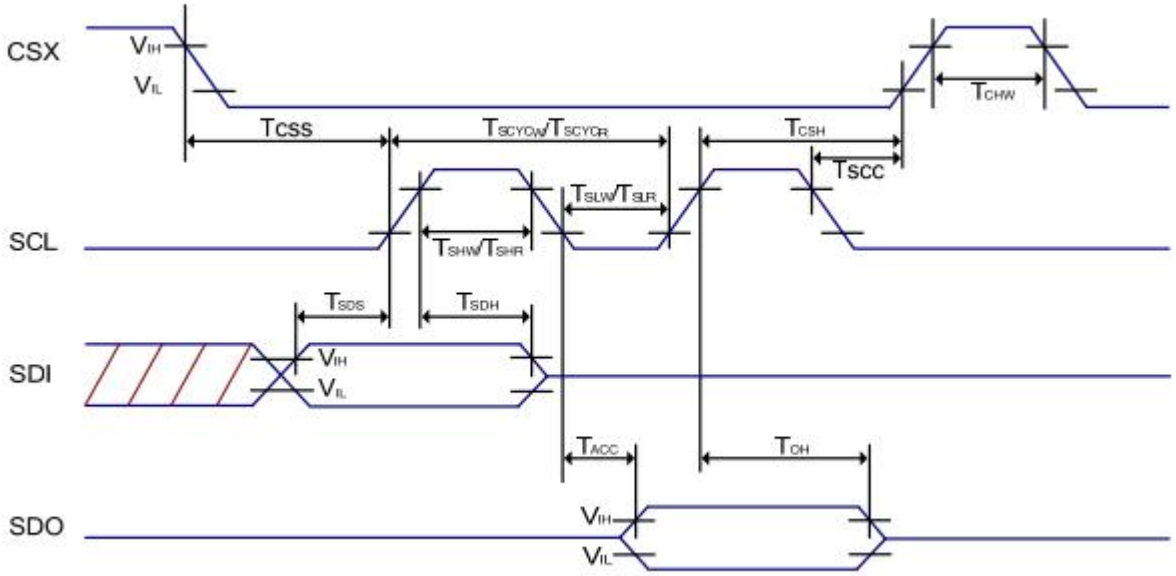


Figure: 3-pin Serial Interface Characteristics

Table: SPI Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time	15	-	ns	-
	T_{CSH}	Chip select hold time	15	-	ns	
	T_{SCC}	Chip select setup time	20	-	ns	
	T_{CHW}	Chip "H" pulse width	40	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66	-	ns	-
	T_{SHW}	SCL "H" pulse width (Write)	10	-	ns	
	T_{SLW}	SCL "L" pulse width (Write)	10	-	ns	
	T_{SCYCR}	Serial clock cycle (Read)	150	-	ns	-
	T_{SHR}	SCL"H" pulse width (Read)	60	-	ns	
	T_{SLR}	SCL"L" pulse width (Read)	60	-	ns	
SDI	TSDS	Data setup time	10	-	ns	-
	T_{SDH}	Data hold time	10	-	ns	
	T_{ACC}	Access time	10	50	ns	For maximum C_L=30pf For minimum C_L=8pf
	T_{OH}	Output disable time	15	50	ns	

Note 1: IOVCC=1.65 to 3.6V, VCI=2.5 to 6V, VSSI=VSS=0V, Ta=-30 to 85℃

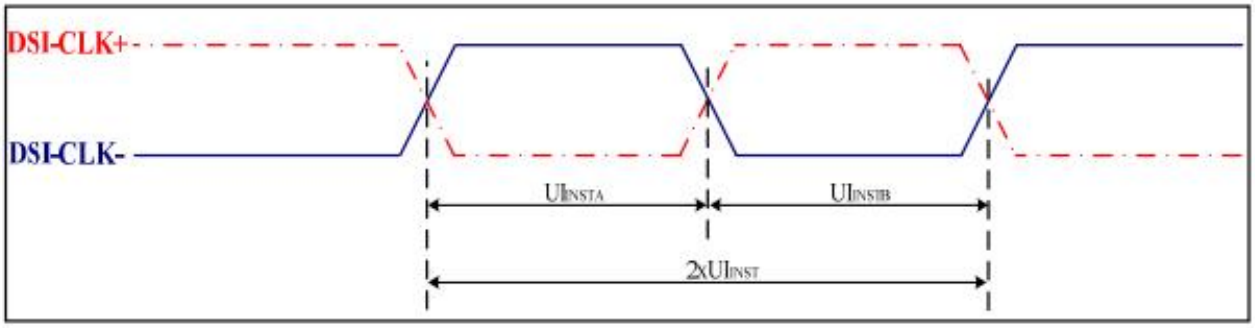
Note 2: The rise time and fall time (tr, tf) of input signal is specified at 15 ns or less.

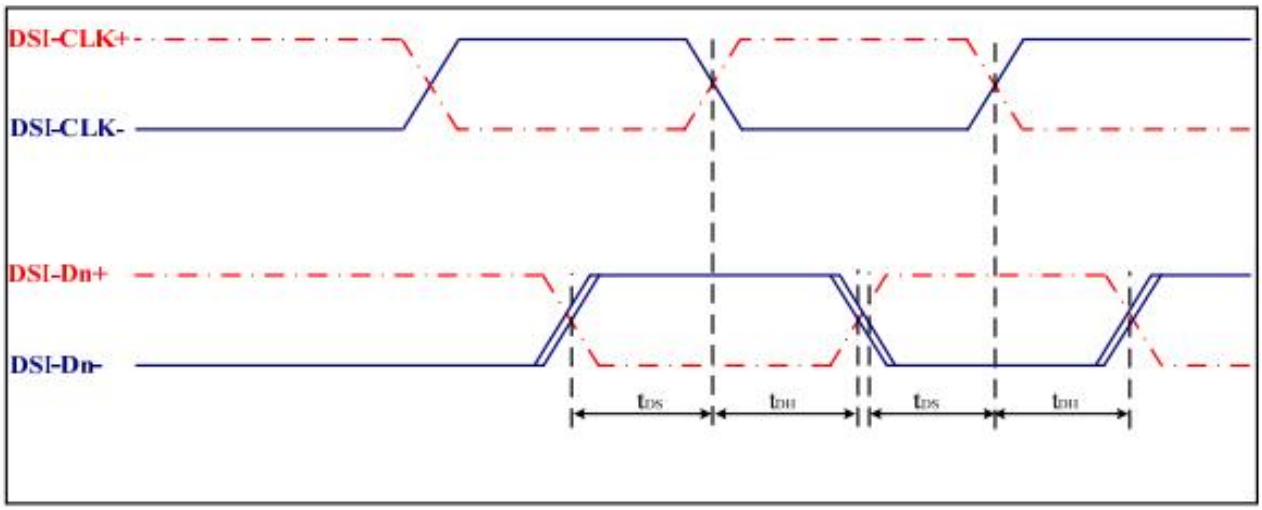
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

7.1.3. MIPI-DSI characteristics

7.1.3.1. High speed mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Mode						
DSI-CLK+/-	$2Xui_{inst}$	Double UI instantaneous	2.22	-	25	ns
DSI-CLK+/-	UI_{INSTA} , UI_{INSTB}	UI instantaneous Halfs	1.11	-	12.5	ns
DSI-Dn+/-	T_{ds}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	T_{dh}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	T_{drclk}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	T_{drdata}	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	T_{dfclk}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	T_{dfdata}	Differential fall time for data	150	-	0.3UI	ps





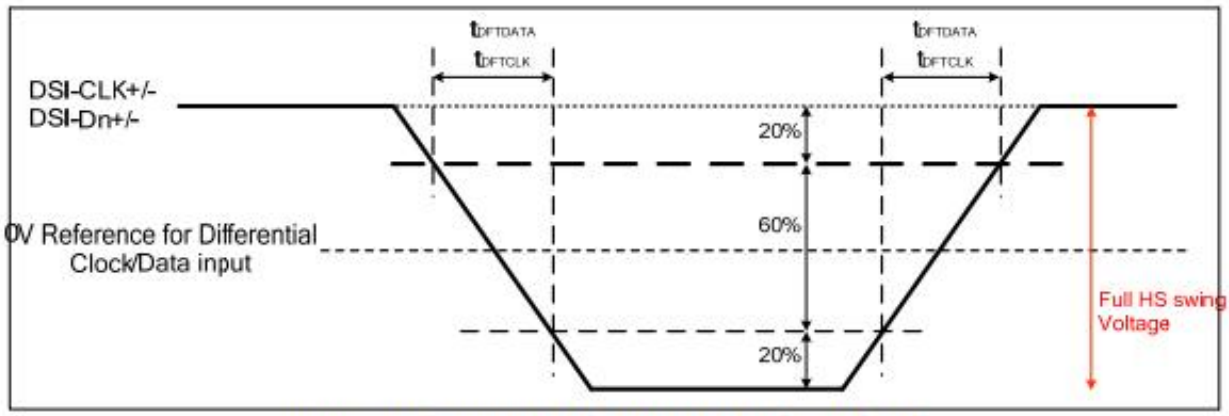


Figure: AC characteristics for MIPI-DSI High speed mode

7.1.3.2. Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power Mode						
DSI-D0+/-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU Display Module	50	-	-	ns
DSI- D0+/-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Modulen MPU	58	-	-	ns
DSI- D0+/-	TTA-SURED	Time-out before the MPU start driving	TLPXD	-	2XTLPXD	ns
DSI- D0+/-	TTA-GETD	Time to drive LP-00 by display module	5XTLPXD	-	-	ns
DSI- D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request – MPU	4XTLPXD	-	-	ns
DSI- D0+/-	Ratio TLPX	Ratio of TLPXM / TLPXD between MCU and display module	2/3	-	3/2	

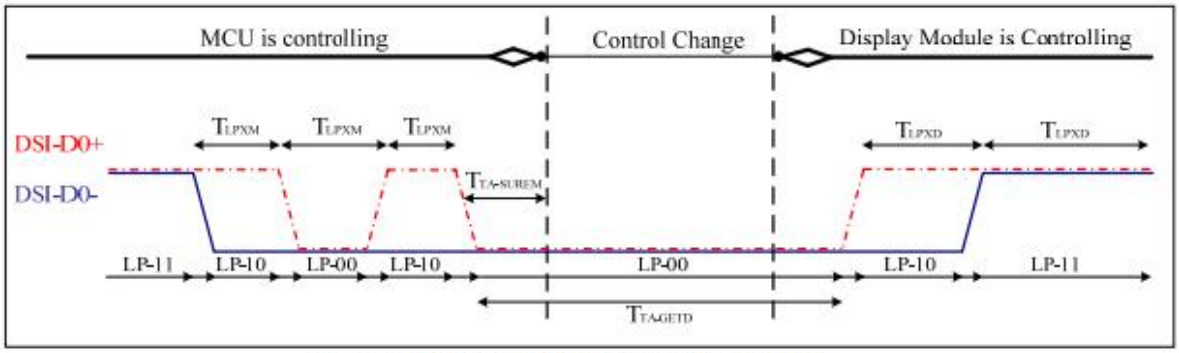


Figure: BTA from the MCU to the Display Module

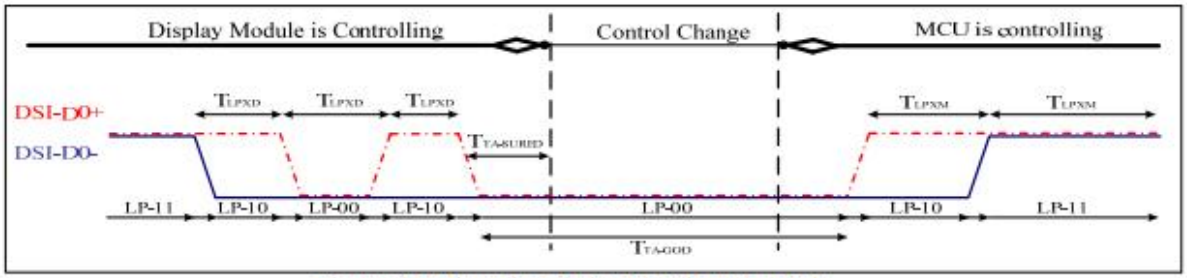


Figure: BTA from the Display Module to the MCU

7.1.3.3. Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	TLPX	Length of any low-power state period	50	-	-	ns
DSI- Dn+/-	THS- PREPARE	Time to drive LP-00 to prepare for HS transmission	40ns+4UI	-	85ns+6UI	ns
DSI- Dn+/-	THS-PREPARE+THS-ZERO	THS-PREPARE+time to drive HS-0 before the sync sequence	145ns+10UI	-	-	ns
DSI- Dn+/-	TD-TERM- EN	Time to enable Data Lane receiver line termination measured from when Dn crosses VIL(max)	Time for Dn to reach VTERM-EN	-	35ns+4UI	ns
DSI- Dn+/-	THS-SKIP	Time-out at RX to ignore transition period of EoT	40	-	55ns+4UI	ns
DSI- Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI- Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns
DSI- Dn+/-	TeoT	Time from start of THS-TRAIL period to start of LP-11 state	-	-	105ns+12UI	ns

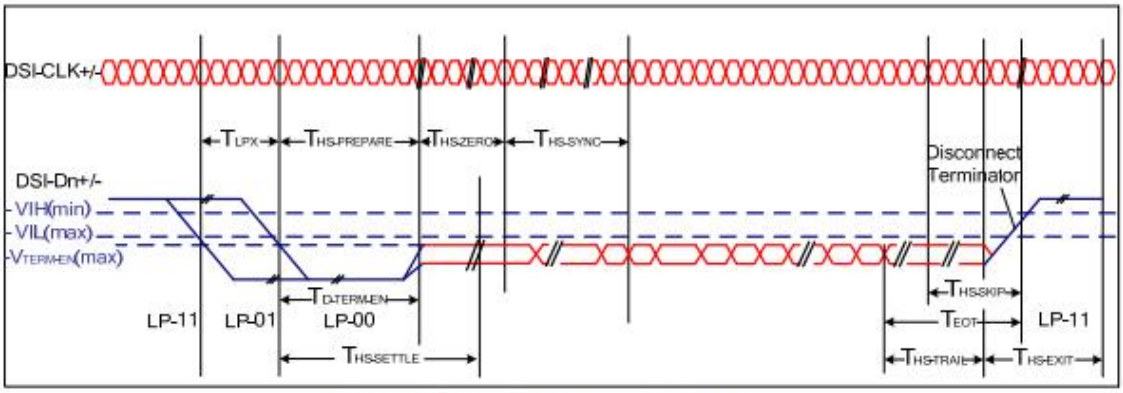


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	TCLK-POST	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns+52UI	-	-	ns
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	TCLK-TERM- EN	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach VTERM-EN	-	38	ns
DSI- CLK+/-	TCLK-PREPARE +TCLK-ZERO	TCLK-PREPARE + time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI- CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	TeoT	Time from start of TCLK-TRAIL period to start of LP-11 state	-	-	105ns+ 12UI	ns

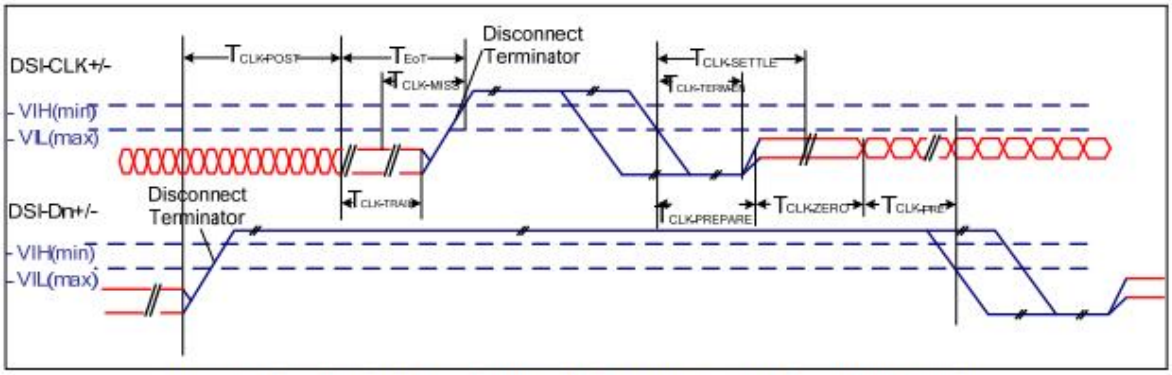


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

8. Inspection Standard

8.1 Incoming Inspection and Standard:

The below incoming inspection are applied to the TFT LCM Modules supplied by ShenZhen Yes-Display International Technology CO.,LTD. The customers should inspect the LCM within 14 days after receiving the goods. The result of inspection should be notified to the Seller in the writing copy promptly, if the customer do not send them within 14 days, the seller has the right to judge as acceptance of goods. The inspection lot size is treated as the quantity per shipment and per model. The sampling plan shall be inspected under MIL-STD015E in Level II by single sampling. The acceptable quality level (AQL) are categorized as below grades:

CRITICAL= 0.4%, MAJOR= 0.65%, MINOR= 1.5%

8.2 Inspection condition and Warranty policy:

The delivered LCM should be stored properly, ideally under climate-controlled environment at 25 (±5) degree Celsius as well as 60% (±10) Relative Humidity. The LCM shall be inspected in the viewing angle of 45 degree from the four major angles (U/D/L/R) under the single fluorescent lamp of 20W (equal to 300 to 500 lux). For warranty, ShenZhen Yes-Display International Technology CO.,LTD. will provide 12 months of warranty period as standard, and provide the new replacement for the defective products which belong to the Seller's responsibility verified by the quality department.

8.3 Inspection Criteria:

8.3.1 Critical defect

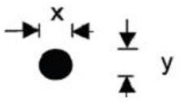
Item No.	Inspection content	Judgement
8.3.1.1	Functional defects	No display, abnormal display, short circuit, missing line, off-contrast and chromaticity, Touch Panel non-function
8.3.1.2	Model mixed	Other model mixed

8.3.2 Major defect:

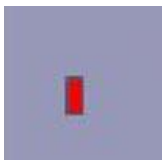
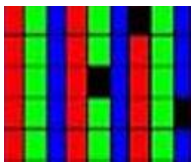
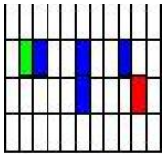
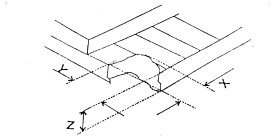
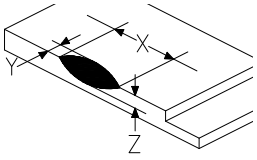
Item No.	Inspection content	Judgement
8.3.2.1	Product indication	Missing model no. and wrong model no. is indicated on the LCM.
8.3.2.2	Glass cracking	The LCD and touch panel glass crack or breakage

8.3.2.3	Missing component	The function component missing such as connector, cable, etc.

8.3.3 Minor defect (LCD) :

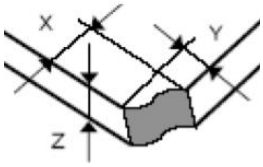
<table>
<tr><th>Item No.</th><th>Inspection content</th><th>Judgement</th></tr>
<tr><td>8.3.3.1</td><td>Black/White spot
Foreign particles
Dust in the cell</td><td>φ=(x+y)/2
 

<table>
<tr><th>Diameter (mm)</th><th>Acceptable Q'ty</th></tr>
<tr><td>Φ ≦ 0.1</td><td>Ignore</td></tr>
<tr><td>0.1 < Φ ≦ 0.25</td><td>3 (Distance>5mm)</td></tr>
<tr><td>0.25 < Φ</td><td>Not allowed</td></tr>
</table></td></tr>
<tr><td>8.3.3.2</td><td>Linear defect
Black/white line
Black/white scratch</td><td>
<table>
<tr><th>Length(mm)</th><th>Width (mm)</th><th>Acceptable Q'ty</th></tr>
<tr><td></td><td>W ≦0.03</td><td>Ignore</td></tr>
<tr><td>L≦ 5.0</td><td>0.03 <W≦0.07</td><td>3</td></tr>
<tr><td></td><td>0.07 <W</td><td>Follow 8.3.3.1</td></tr>
</table></td></tr>
<tr><td>8.3.3.3</td><td>Polarizer Bubbles
Dent on polarizer</td><td>
<table>
<tr><th>Diameter (mm)</th><th>Acceptable Q'ty</th></tr>
<tr><td>Φ ≦ 0.2</td><td>Ignore</td></tr>
<tr><td>0.2 < Φ ≦ 0.5</td><td>2 (Distance>5mm)</td></tr>
<tr><td>0.5 < Φ</td><td>Not allowed</td></tr>
</table></td></tr>
</table>

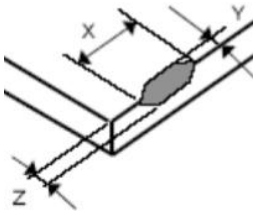
<table>
<tr>
<td>8.3.3.4</td>
<td>Electrical Dot defect</td>
<td>
Bright dot and Dark dot definition:
 or 
 (Two adjacent dot)
Inspection pattern: black, white, red, green, and blue screen.
<table>
<tr><th>Items</th><th>Acceptable Q'ty</th></tr>
<tr><td>Bright dot</td><td>N ≦ 4 (Distance >5mm)</td></tr>
<tr><td>Dark dot</td><td>N ≦ 4 (Distance >5mm)</td></tr>
</table>
</td>
</tr>
<tr>
<td>8.3.3.5</td>
<td>Glass Defect-Corner chipping</td>
<td>

<table>
<tr><th>Size(mm)</th><th>Judgement</th></tr>
<tr><td>X≦3mm, Y≦S ,
Z≦ T
(S= ITO length, T=Single glass thickness)</td><td>Accept</td></tr>
</table>
</td>
</tr>
<tr>
<td>8.3.3.6</td>
<td>Glass Defect-Side fragment</td>
<td>

<table>
<tr><th>Size(mm)</th><th>Judgement</th></tr>
<tr><td>X≦2 mm, Y≦ border edge
Z≦T
(T= single glass thickness)</td><td>Accept</td></tr>
</table>
</td>
</tr>
</table>

8.3.4 Minor defect (Touch Panel)

Item No.	Inspection content	Judgement

<table>
<tr><td>8.3.4.1</td><td>Scratch, dust, particles, foreign materials in “linear type”</td><td>
<table>
<tr><th>Size (mm)</th><th>Acceptable Q’ty</th></tr>
<tr><td>W≦0.05mm, L≦10mm</td><td>Ignore</td></tr>
<tr><td>0.05mm<W ≦ 0.07mm, L ≦ 10mm</td><td>3</td></tr>
<tr><td>W>0.07mm</td><td>Reject</td></tr>
</table>
</td></tr>
<tr><td>8.3.4.2</td><td>Scratch, dust, particles, foreign materials in “round type”</td><td>
<table>
<tr><th>Diameter (mm)</th><th>Acceptable Q’ty</th></tr>
<tr><td>Φ≦ 0.25mm</td><td>Ignore</td></tr>
<tr><td>0.25mm<Φ≦ 0.35mm</td><td>5</td></tr>
<tr><td>Φ > 0.35mm</td><td>Reject</td></tr>
</table>
</td></tr>
<tr><td>8.3.4.3</td><td>Air bubbles</td><td>
<table>
<tr><th>Diameter (mm)</th><th>Acceptable Q’ty</th></tr>
<tr><td>Φ≦ 0.2mm</td><td>Ignore</td></tr>
<tr><td>0.2mm<Φ≦ 0.5mm</td><td>3</td></tr>
<tr><td>Φ > 0.5mm</td><td>Reject</td></tr>
</table>
</td></tr>
<tr><td>8.3.4.5</td><td>Scratch on printing area</td><td>
<table>
<tr><th>Size (mm)</th><th>Acceptable Q’ty</th></tr>
<tr><td>W≦0.03mm, L≦5 mm</td><td>Ignore</td></tr>
<tr><td>0.03mm<W≦0.05mm, L≦5mm</td><td>3</td></tr>
<tr><td>W>0.05mm or L> 5mm</td><td>Reject</td></tr>
</table>
</td></tr>
<tr><td>8.3.4.6</td><td>Corner chipping</td><td>


<table>
<tr><th>Size(mm)</th><th>Judgement</th></tr>
<tr><td>X≦2mm, Y≦2mm
Z<1/2T
(T= single glass thickness)</td><td>Accept</td></tr>
</table>
</td></tr>
</table>

8.3.4.7	Edge chipping	

Size(mm)	Judgement
X≦3 mm, Y≦3 mm Z≦1/2 T (T= single glass thickness)	Accept

9. Reliability Test Conditions and Methods

9.1 Reliability Test Conditions and Methods:

NO.	TEST ITEMS	TEST CONDITION	INSPECTION AFTER TEST
①	High Temperature Storage	80°C±2°C×96Hours	Inspection after 2~4hours storage at room temperature, the samples should be free from defects: 1, Air bubble in the LCD. 2, Seal leak. 3, Non-display. 4, Missing segments. 5, Glass crack. 6, Current IDD is twice higher than initial value. 7, The surface shall be free from damage. 8, The electric characteristic requirements shall be satisfied.
②	Low Temperature Storage	-30°C±2°C×96Hours	
③	High Temperature Operating	70°C±2°C×96Hours	
④	Low Temperature Operating	-20°C±2°C×96Hours	
⑤	Temperature Cycle(Storage)	-20°C ⟺ 25°C ⟺ 70°C (30min) (5min) (30min) 1cycle Total 10cycle	
⑥	Damp Proof Test (Storage)	50°C±5°C×90%RH×96Hours	
⑦	Vibration Test	Frequency:10Hz~55Hz~10Hz Amplitude:1.5MM X,Y,Z direction for total 3hours (packing condition test will be tested by a carton)	
⑧	Drooping Test	Drop to the ground from 1M height one time every side of carton. (packing condition test will be tested by a carton)	
⑨	ESD Test	Voltage:±8KV,R:330Ω,C:150PF,Air Mode,10times	

REMARK:

1, The Test samples should be applied to only one test item.

2, Sample side for each test item is 5~10pcs.

3,For Damp Proof Test, Pure water(Resistance＞10MΩ)should be used.

4,In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.

5, EL evaluation should be accepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.

6, Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

10. Cautions and Handling Precautions

10.1 Mounting method

The LCD panel of TFT module consists of two thin glass plates with polarizes which easily be damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board.

Extreme care should be needed when handling the LCD modules.

10.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent

[Recommended below] and wipe lightly

- Isopropyl alcohol
- Ethyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns

Do not use the following solvent on the pad or prevent it from being contaminated:

- Soldering flux
- Chlorine (Cl) , Sulfur (S)

If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.

If ITO corrosion happen by miss-handling or using some materials such as Chlorine (CI), Sulfur (S) from customer, Responsibility is on customer.

10.3 Caution against static charge

The LCD module use C-MOS LSI drivers, so we recommended that you:

Connect any unused input terminal to power or ground, do not input any signals before power is turned on, and ground your body, work/assembly areas, and assembly equipment to protect against static electricity.

10.4 packing

- Module employs LCD elements and must be treated as such.
- Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity

10.5 Caution for operation

- It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage then the limit cause the shorter LCD life.
- An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.
- Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature LCD's how dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.
- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- Slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.

Usage under the maximum operating temperature, 50%Rh or less is required.

10.6 storing

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

- Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.
- Storing with no touch on polarizer surface by the anything else.

[It is recommended to store them as they have been contained in the inner container at the time of delivery from us

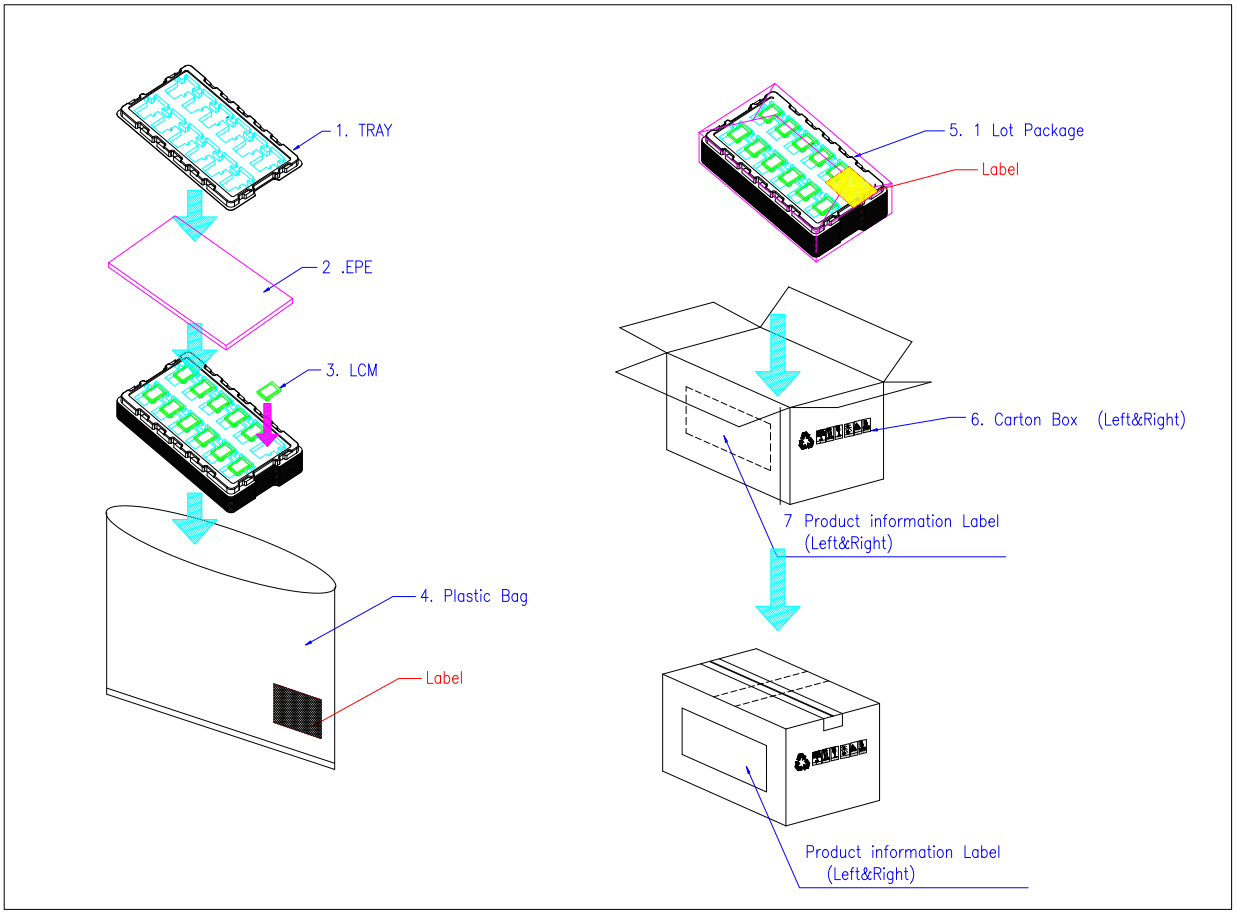
10.7 Safety

- It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.

- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water

11. Packing Method

11.1 Method



11.2 Packing Label

TBD